

**Amendments to the Claims****Listing of Claims:**

5      Claims 1-13 (cancelled)

Claim 14 (Currently Amended) : An apparatus for adjusting a phase difference

between two input signals, the apparatus comprising:

- 10     a first buffer for buffering a first input signal and outputting a first output signal;
- 15     a first DAC for outputting a first control voltage corresponding to a first digital value representative of a phase delay;
- 20     a first variable capacitor coupled to the first DAC and the first buffer, the capacitance value of the first variable capacitor corresponding to the first control voltage;
- 25     a second buffer for buffering a second input signal and outputting a second output signal;
- 30     a second DAC for outputting a second control voltage corresponding to a second digital value representative of a phase delay; and
- 35     a second variable capacitor coupled to the second DAC and the second buffer, the capacitance value of the second variable capacitor corresponding to the second control voltage;
- 40     wherein by controlling at least one of the first and the second digital values, the phase difference between the first input signal and the second input signal ~~are~~ is adjusted.

Claim 15 (previously presented) : The apparatus of claim 14 being implemented in a receiver.

- 45     Claim 16 (previously presented) : The apparatus of claim 14 being implemented in a transmitter.

Claim 17 (previously presented) : The apparatus of claim 14 being implemented in a transceiver.

5 Claim 18 (previously presented) : The apparatus of claim 14, wherein the first input signal and the second input signal are differential signals.

10 Claim 19 (previously presented) : The apparatus of claim 14, wherein the first input signal and the second input signal are an in-phase signal and a quadrature-phase signal respectively.

Claim 20 (previously presented) : The apparatus of claim 14, wherein the first input signal and the second input signals are clock signals.

15 Claim 21 (previously presented) : The apparatus of claim 14, wherein the first input signal and the second input signal are RF signals.

20 Claim 22 (previously presented) : The apparatus of claim 14, wherein the first variable capacitor and the second variable capacitor are voltage-controlled capacitors.

Claim 23 (previously presented) : The apparatus of claim 22, wherein the voltage-controlled capacitors are MOS-based voltage-controlled capacitors.

25 Claim 24 (previously presented) : The apparatus of claim 22, wherein the voltage-controlled capacitors are P+/N well junction voltage-controlled capacitors.

30 Claim 25 (Currently Amended) : A method for adjusting a phase difference between two input signals, the method comprising:  
buffering a first input signal and outputting a first output signal;

buffering a second input signal and outputting a second output signal;  
providing at least one of a first digital value and a second digital value

representative of a first phase delay and a second phase delay  
respectively; and

5       adjusting at least one of a capacitance value of a first variable capacitor with  
a first control voltage generated from the first digital value or adjusting  
and a capacitance value of a second variable capacitor with a second  
control voltage generated from the second digital value, to adjust the  
phase difference between the input signal and the output signal.

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Claim 26 (previously presented) : The method of claim 25, wherein the first input  
signal and the second input signal are differential signals.

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Claim 27 (previously presented) : The method of claim 25, wherein the first input  
signal and the second input signal are an in-phase signal and a  
quadrature-phase signal respectively.

Claim 28 (previously presented) : The method of claim 25, wherein the first input  
signal and the second input signals are clock signals.

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Claim 29 (previously presented) : The method of claim 25, wherein the first input  
signal and the second input signal are RF signals.

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Claim 30 (previously presented) : The method of claim 25, wherein the first  
variable capacitor and the second variable capacitor are voltage-controlled  
capacitors.

Claim 31 (previously presented) : The method of claim 30, wherein the  
voltage-controlled capacitors are MOS-based voltage-controlled capacitors.

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Claim 32 (previously presented) : The method of claim 30, wherein the

voltage-controlled capacitors are P+/N well junction voltage-controlled capacitors.

Claim 33 ( new ) : An apparatus for adjusting a phase difference between an  
5 in-phase signal and a quadrature-phase signal, the apparatus comprising:  
a first adjusting circuit, the first adjusting circuit comprising:  
a first buffer for buffering the in-phase signal and outputting a first output  
signal;  
a first DAC for outputting a first control voltage corresponding to a first  
10 digital value representative of a phase delay; and  
a first variable capacitor coupled to the first DAC and the first buffer, the  
capacitance value of the first variable capacitor corresponding to the  
first control voltage; and  
a second adjusting circuit, the second adjusting circuit comprising:  
15 a second buffer for buffering the quadrature-phase signal and outputting a  
second output signal;  
a second DAC for outputting a second control voltage corresponding to a  
second digital value representative of a phase delay; and  
a second variable capacitor coupled to the second DAC and the second  
20 buffer, the capacitance value of the second variable capacitor  
corresponding to the second control voltage;  
wherein by controlling at least one of the first and the second adjusting  
circuit, the phase difference between the in-phase signal and the  
quadrature-phase signal reaches a predetermined condition.

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Claim 34 ( new ) : An apparatus for adjusting a phase difference between a positive  
signal of a differential signal and a negative signal of the differential signal,  
the apparatus comprising:

30 a first adjusting circuit, comprising:  
a first buffer for buffering the positive signal and outputting a first output  
signal;

a first DAC for outputting a first control voltage corresponding to a first digital value representative of a phase delay; and  
5 a first variable capacitor coupled to the first DAC and the first buffer, the capacitance value of the first variable capacitor corresponding to the first control voltage; and  
a second adjusting circuit, comprising:  
a second buffer for buffering the negative signal and outputting a second output signal;  
10 a second DAC for outputting a second control voltage corresponding to a second digital value representative of a phase delay; and  
a second variable capacitor coupled to the second DAC and the second buffer, the capacitance value of the second variable capacitor corresponding to the second control voltage;  
wherein by controlling at least one of the first and the second adjusting  
15 circuit, the phase difference between the positive signal and the negative signal reaches a predetermined condition.

Claim 35 (new): A method for adjusting a phase difference between an in-phase signal and a quadrature-phase signal, the method comprising:  
20 buffering the in-phase signal and outputting a first output signal;  
buffering the quadrature-phase signal and outputting a second output signal;  
providing at least one of a first digital value and a second digital value  
representative of a first phase delay and a second phase delay  
respectively; and  
25 adjusting at least one of a first variable capacitor and a second variable capacitor by respectively utilizing a first control voltage generated from the first digital value and a second control voltage generated from the second digital value, to make the phase difference between the in-phase signal and the quadrature-phase signal reach a predetermined  
30 condition.

Claim 36 (new): A method for adjusting a phase difference between a positive

signal of a differential signal and a negative signal of the differential signal,  
the method comprising:

buffering the positive signal and outputting a first output signal;

buffering the negative signal and outputting a second output signal;

5 providing at least one of a first digital value and a second digital value

representative of a first phase delay and a second phase delay

respectively; and

adjusting at least one of a first variable capacitor and a second variable  
capacitor by respectively utilizing a first control voltage generated

10 from the first digital value and a second control voltage generated from  
the second digital value, to have the phase difference between the  
positive signal and the negative signal reach a predetermined  
condition.

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